Atty. Dkt. No. 045054-0158

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hitoshi IRINO

Title: SEMICONDUCTOR PROTECTION ELEMENT, SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME

Appl. No.: 10/796,999

Filing Date: 03/11/2004

Examiner: Unassigned

Art Unit: Unassigned

TRANSMITTAL OF FORMAL DRAWINGS

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

ATTENTION: DRAWING REVIEW BRANCH

Sir:

Transmitted herewith are the formal drawings (16 sheets, Figures 1-2, 3A-3B, 4A-4B, 5-28, 29A-29B) for the above-identified application. The Official Draftsperson is respectfully requested to approve these drawings for entry into the application.

Respectfully submitted,

Date: April 30, 2004

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for David A. Blumenthal
Attorney for Applicant
Registration No. 26,257

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Facsimile: (202) 672-5399

FIG.1

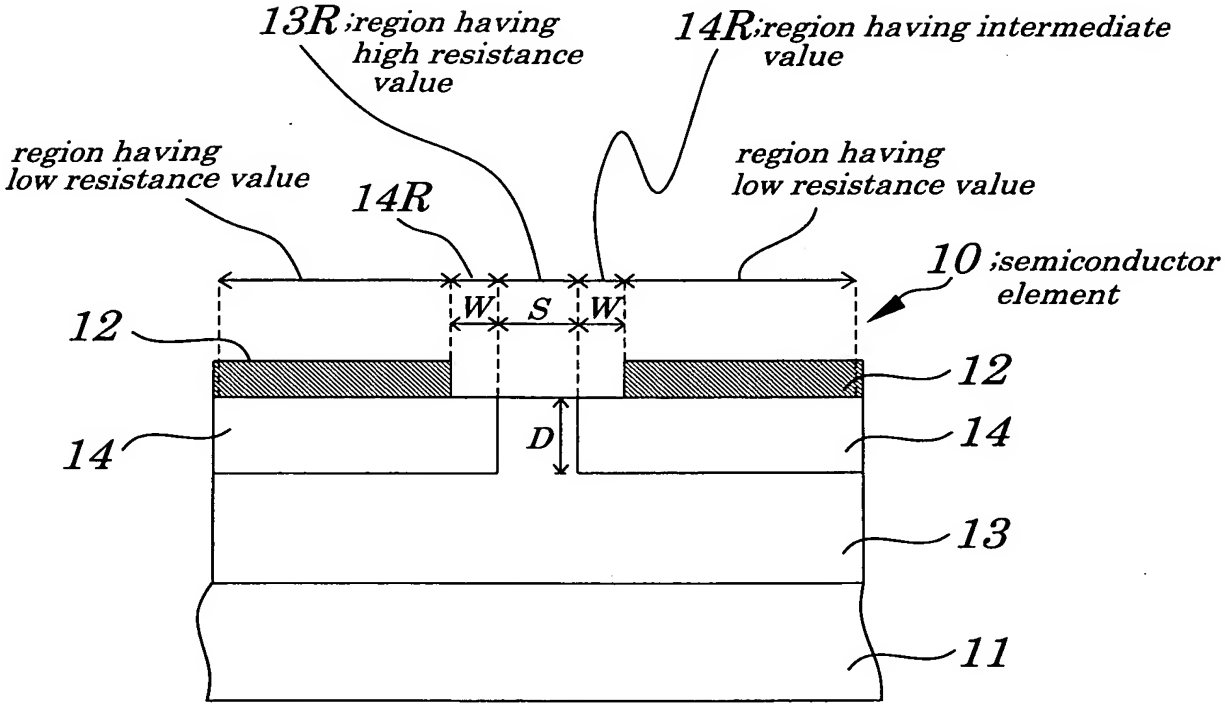

FIG.2

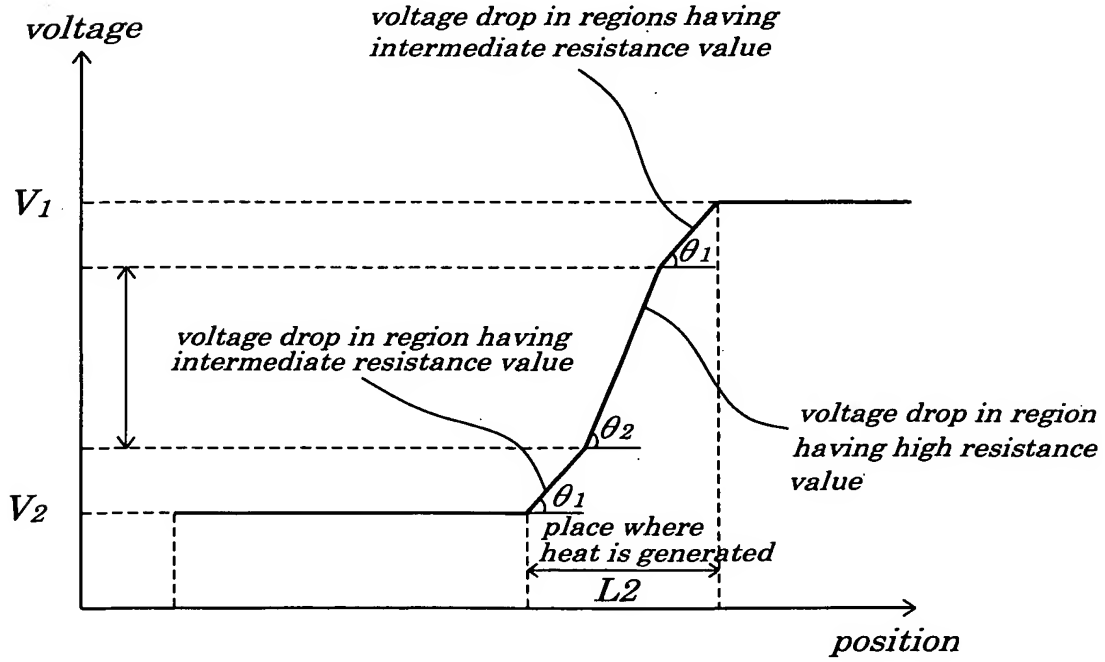

FIG. 3A (PRIOR ART)

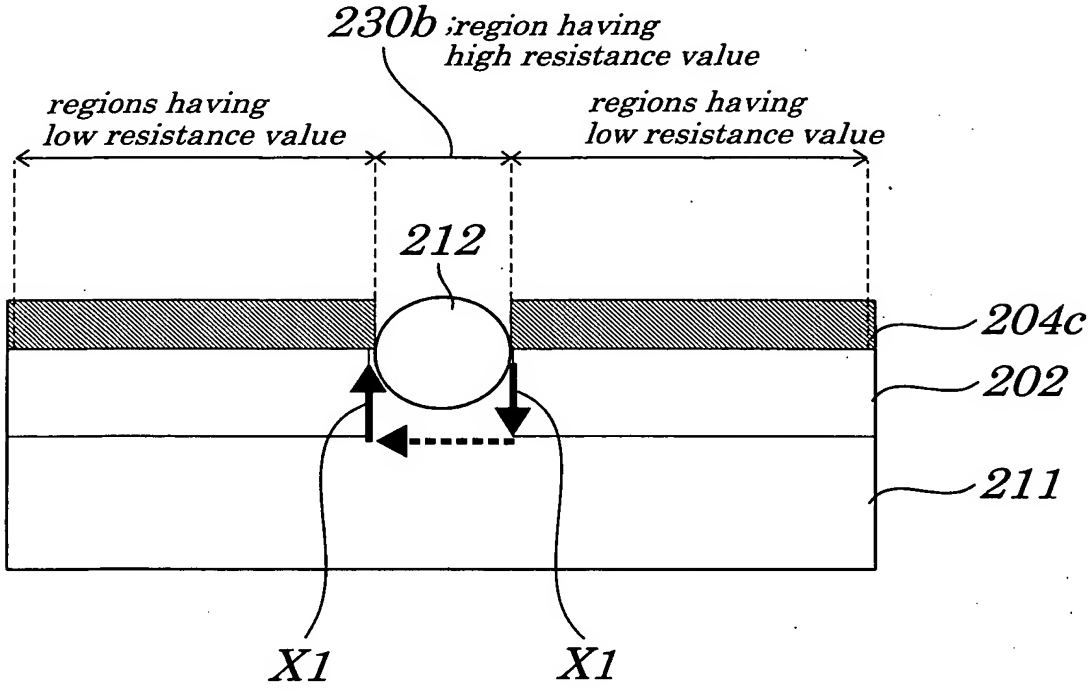

FIG. 3B

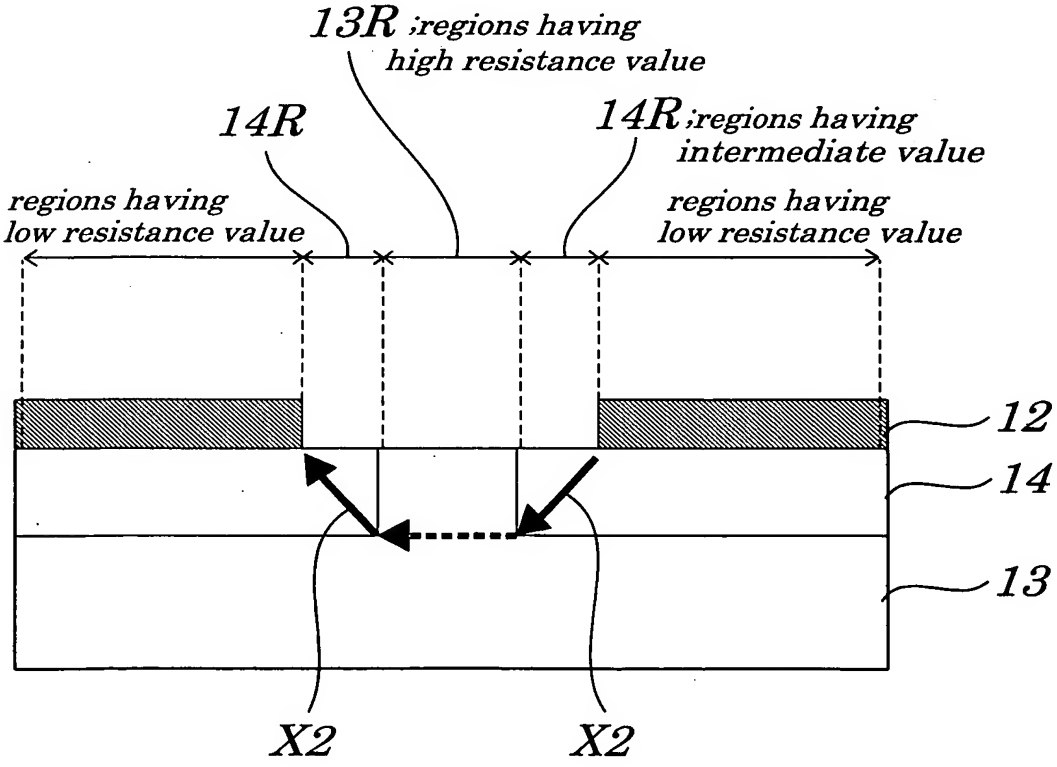

FIG. 4A

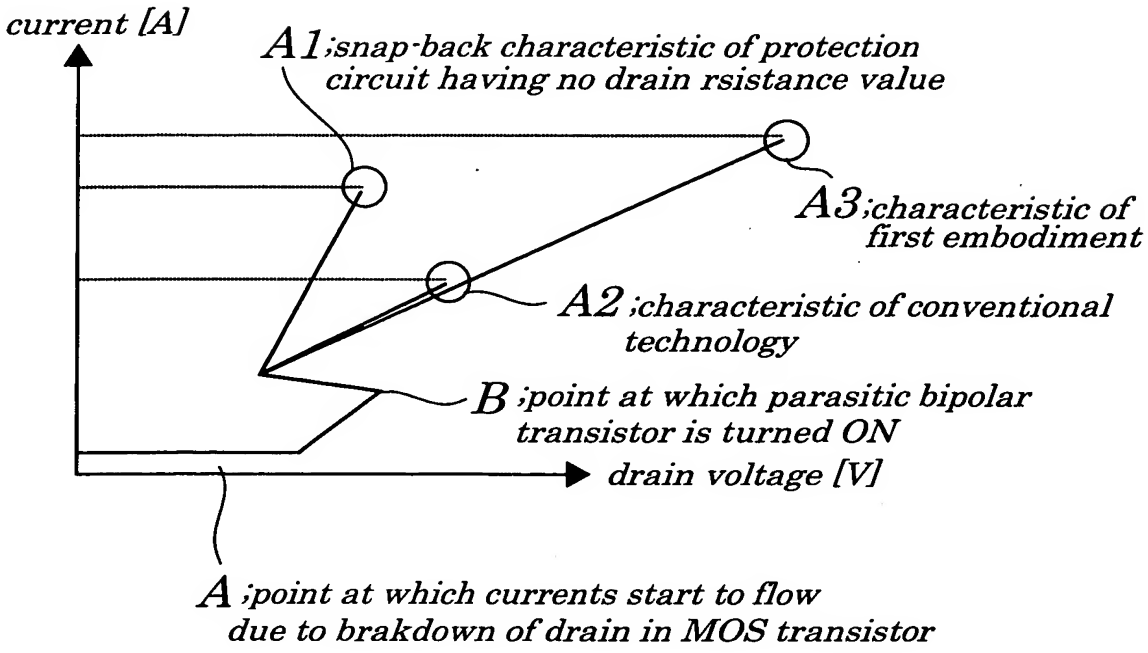
current [A]
A1;snap-back characteristic of protection circuit having no drain rsistance value
A3;characteristic of first embodiment
A2;characteristic of conventional technology
B;point at which parasitic bipolar transistor is turned ON
drain voltage [V]
A;point at which currents start to flow due to brakdown of drain in MOS transistor

FIG. 4B

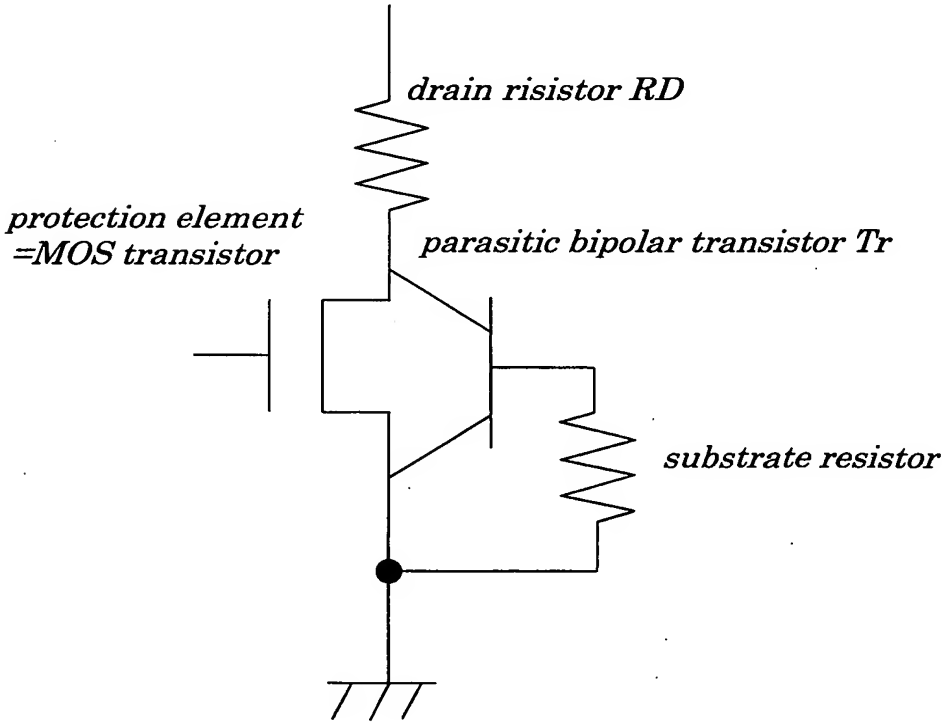
drain risistor RD
protection element =MOS transistor
parasitic bipolar transistor Tr
substrate resistor

FIG.5

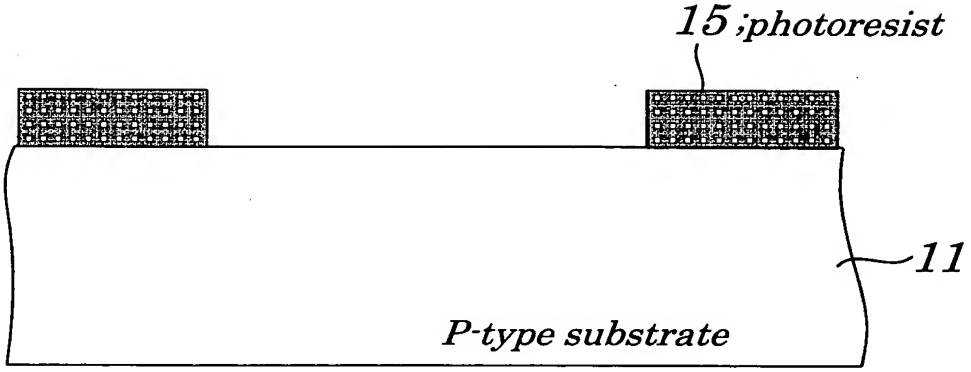
15 ;photoresist
11
P-type substrate

FIG.6

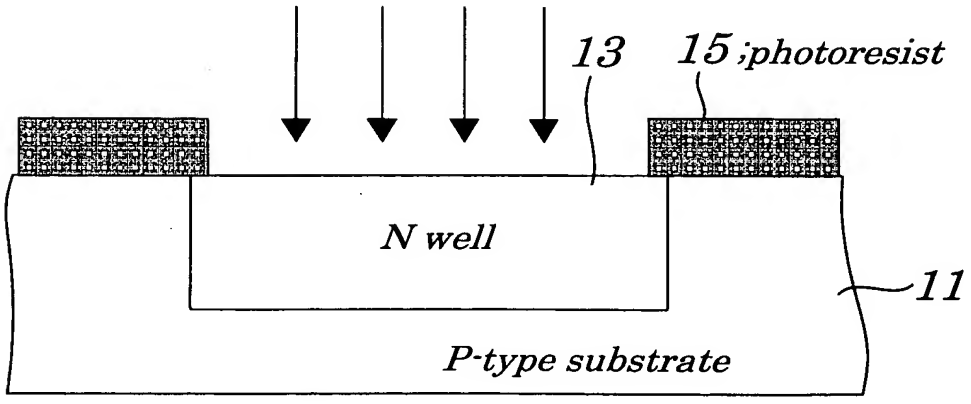
13
15 ;photoresist
N well
11
P-type substrate

FIG. 7

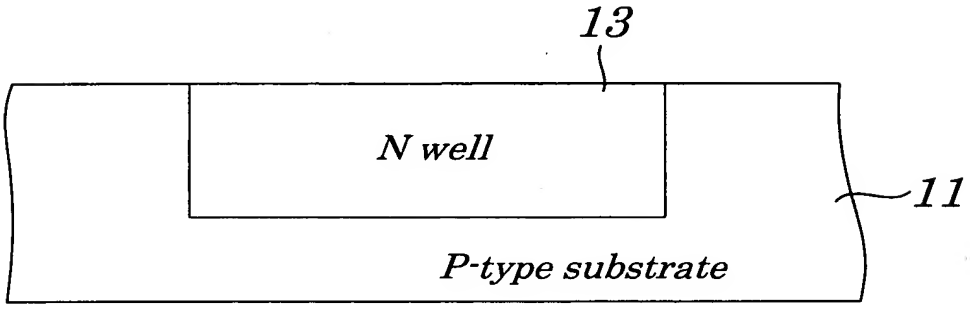
13
N well
11
P-type substrate

FIG. 8

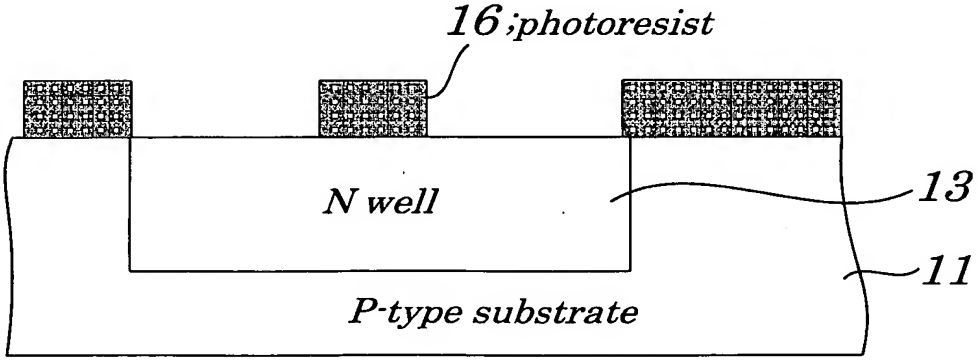
16;photoresist
N well
13
11
P-type substrate

FIG.9

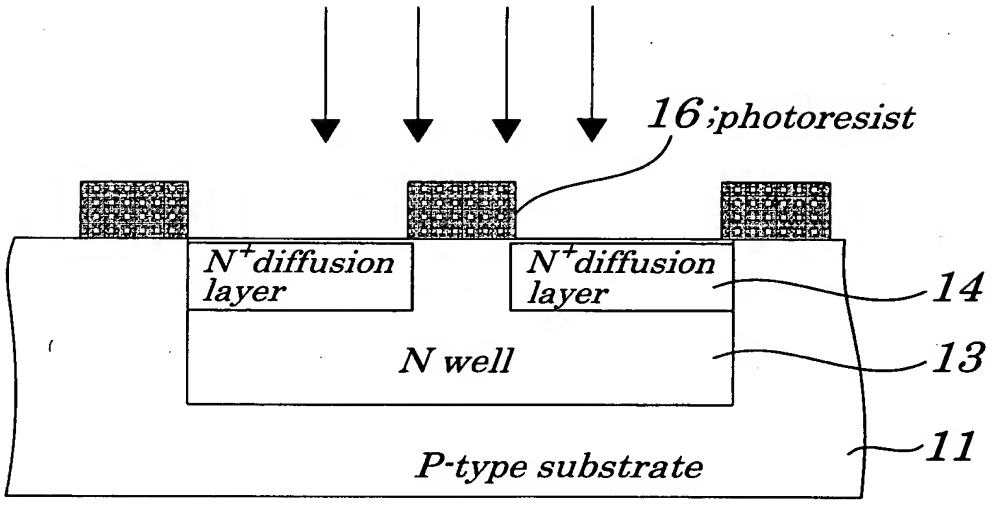
16 ;photoresist
N+diffusion layer
N+diffusion layer
14
N well
13
11
P-type substrate

FIG.10

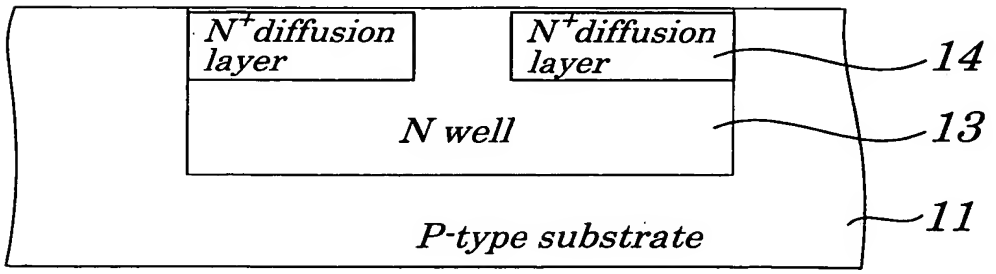
N+diffusion layer
N+diffusion layer
14
N well
13
11
P-type substrate

FIG.11

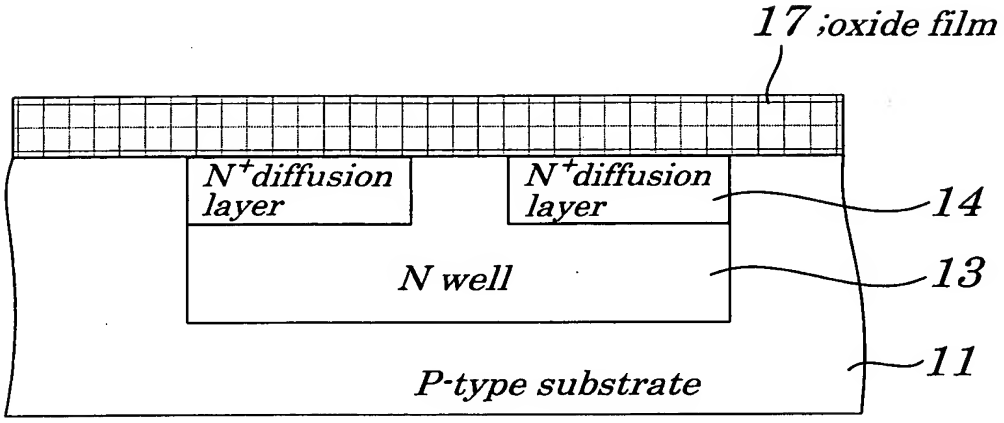
17 ;oxide film
N+diffusion layer
N+diffusion layer
14
N well
13
11
P-type substrate

FIG.12

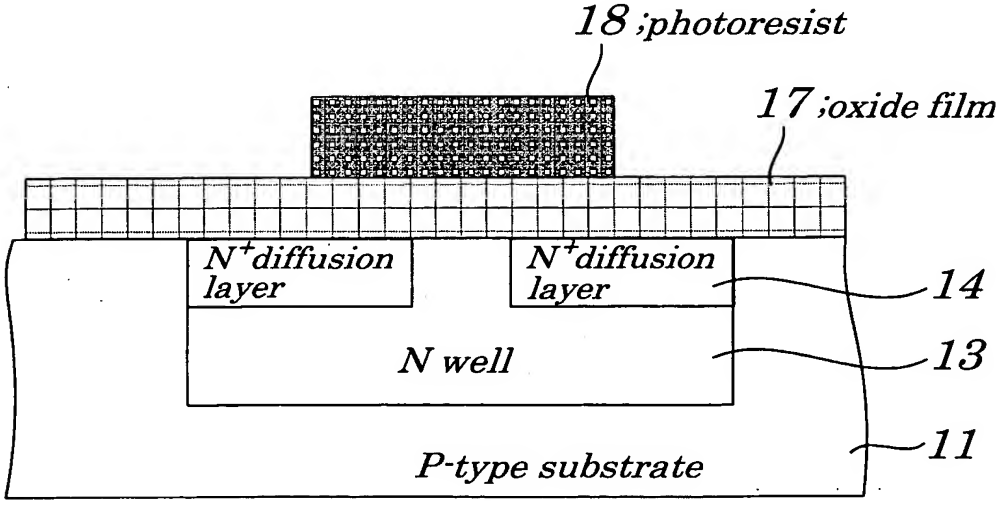
18 ;photoresist
17 ;oxide film
N+diffusion layer
N+diffusion layer
14
N well
13
11
P-type substrate

FIG.13

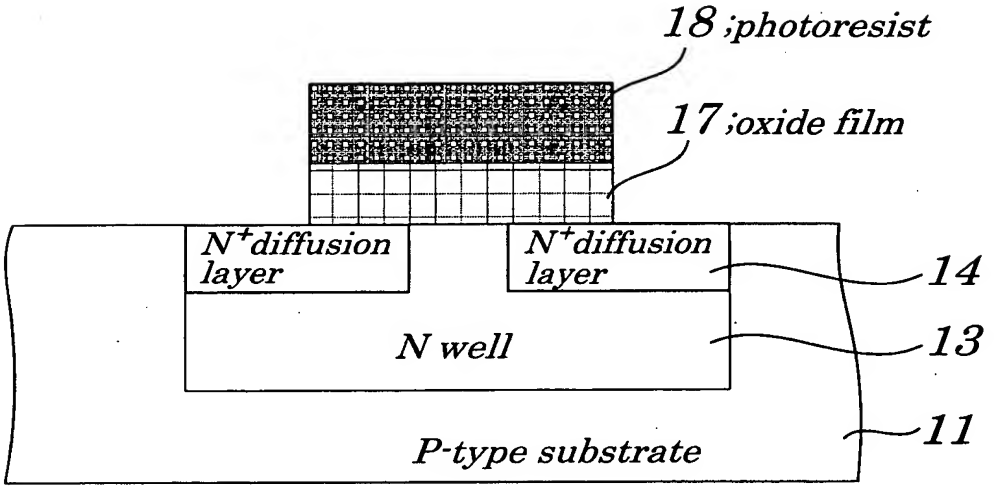
18 ;photoresist
17 ;oxide film
N+diffusion layer
N+diffusion layer
14
N well
13
11
P-type substrate

FIG.14

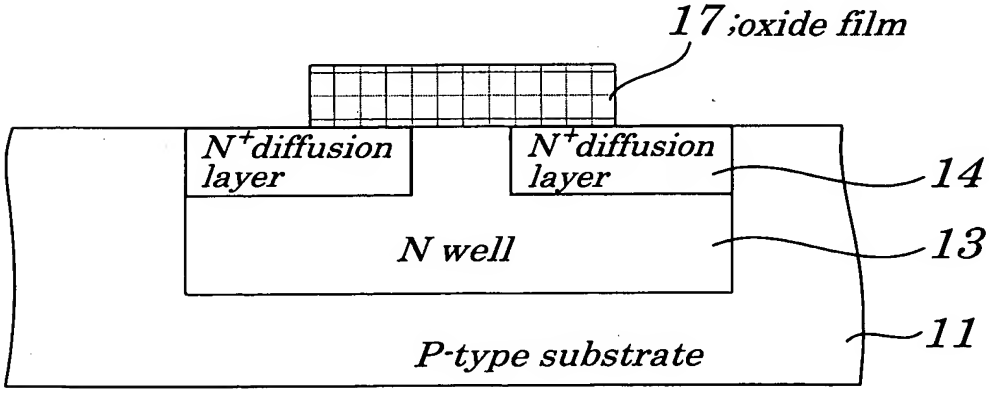
17 ;oxide film
N+diffusion layer
N+diffusion layer
14
N well
13
11
P-type substrate

FIG.15

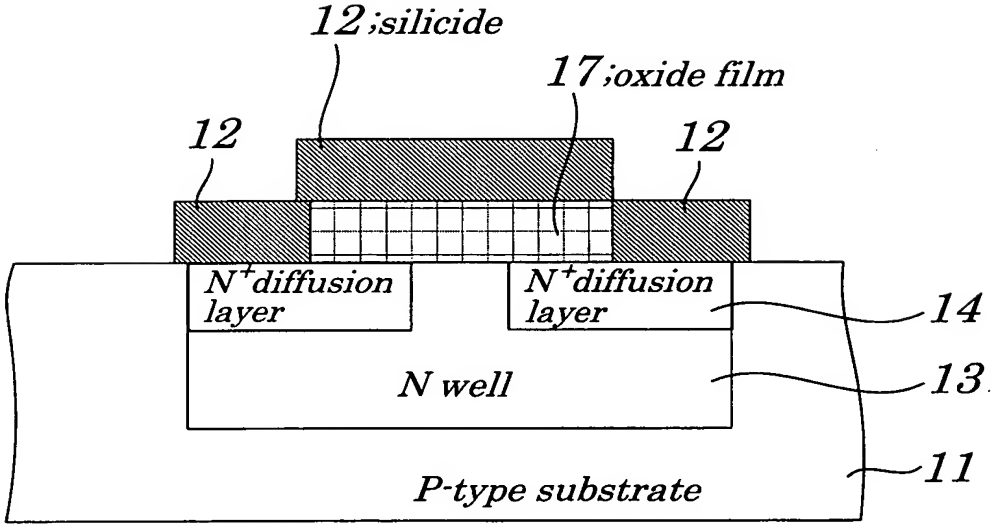
12;silicide
17;oxide film
12
12
N+diffusion layer
N+diffusion layer
14
N well
13
P-type substrate
11

FIG.16

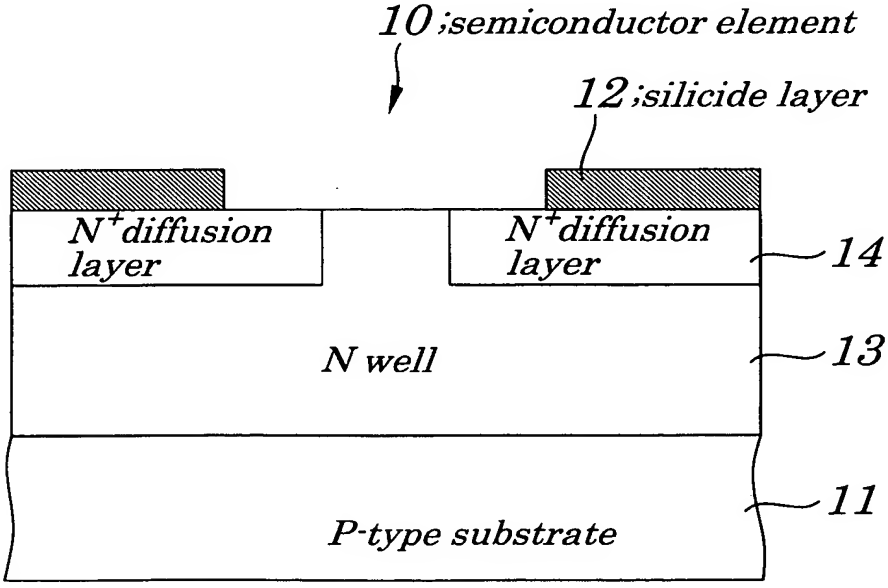
10;semiconductor element
12;silicide layer
N+diffusion layer
N+diffusion layer
14
N well
13
P-type substrate
11

FIG.17

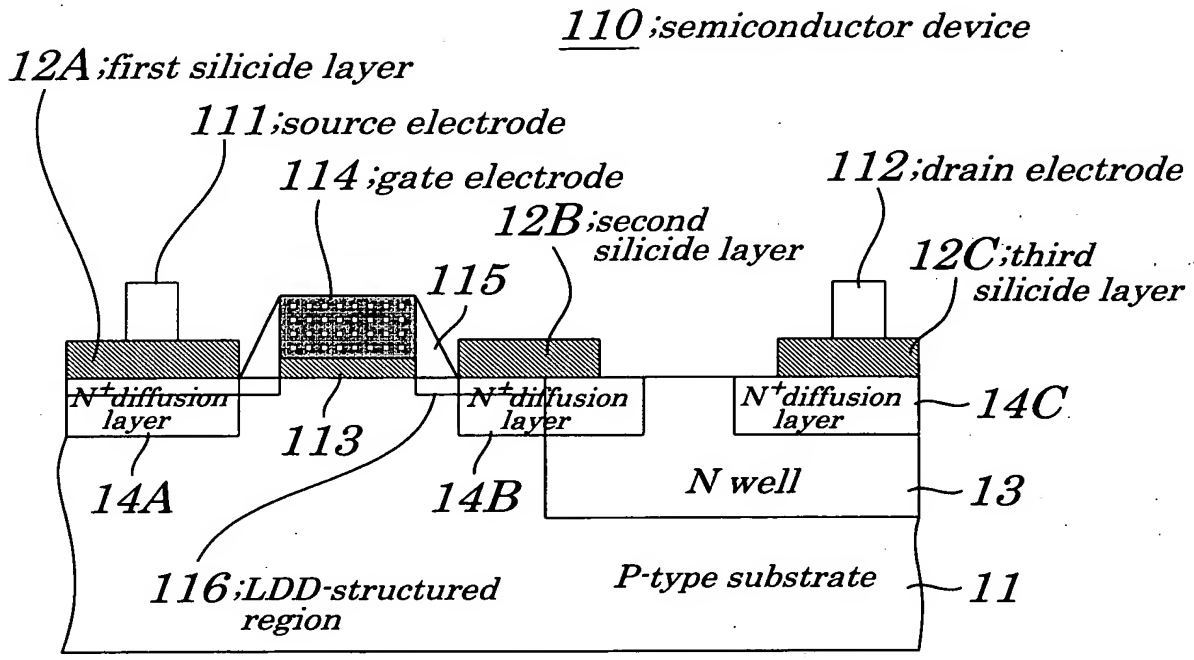
110;semiconductor device
12A;first silicide layer
111;source electrode
114;gate electrode
112;drain electrode
12B;second silicide layer
12C;third silicide layer
115
N+diffusion layer
N+diffusion layer
N+diffusion layer
14C
113
14A
14B
N well
13
116;LDD-structured region
P-type substrate
11

FIG.18

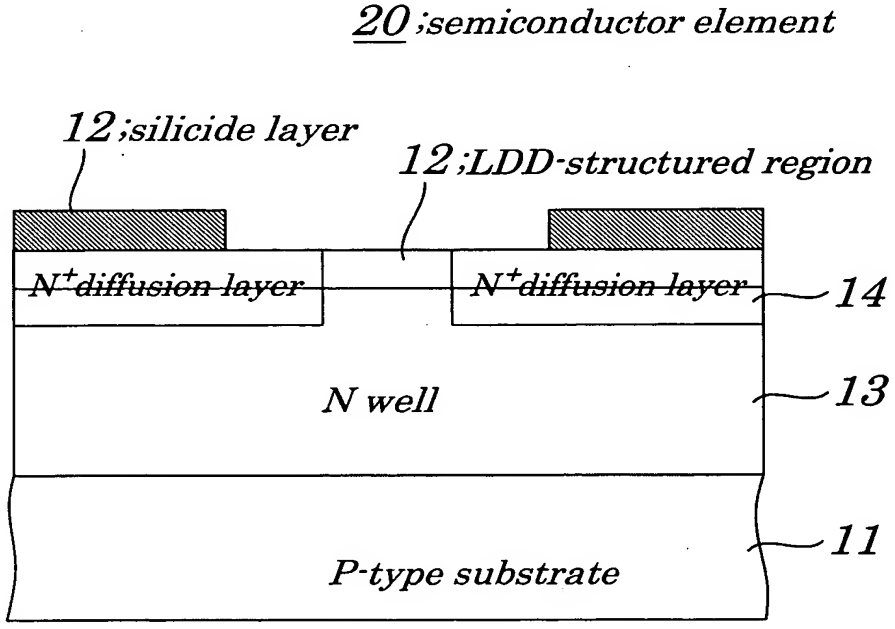
20;semiconductor element
12;silicide layer
12;LDD-structured region
N+diffusion layer
N+diffusion layer
14
N well
13
11
P-type substrate

FIG.19

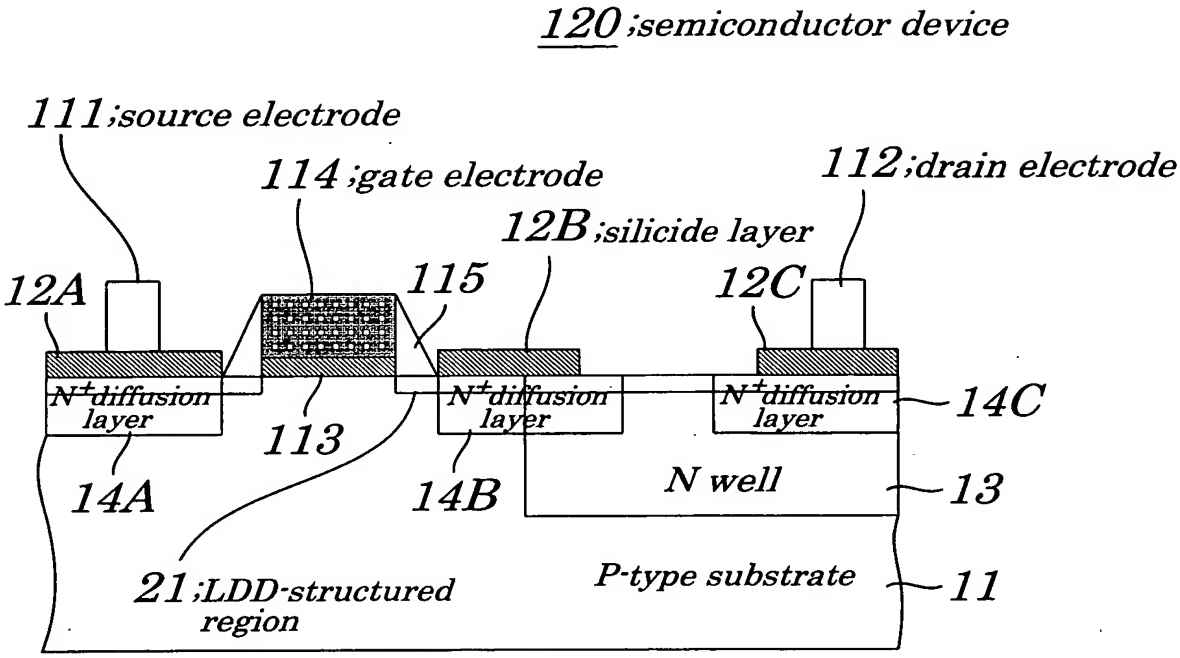
120;semiconductor device
111;source electrode
114;gate electrode
112;drain electrode
12B;silicide layer
12A
115
12C
N+diffusion layer
N+diffusion layer
N+diffusion layer
14C
113
14A
14B
N well
13
21;LDD-structured region
P-type substrate
11

FIG.20

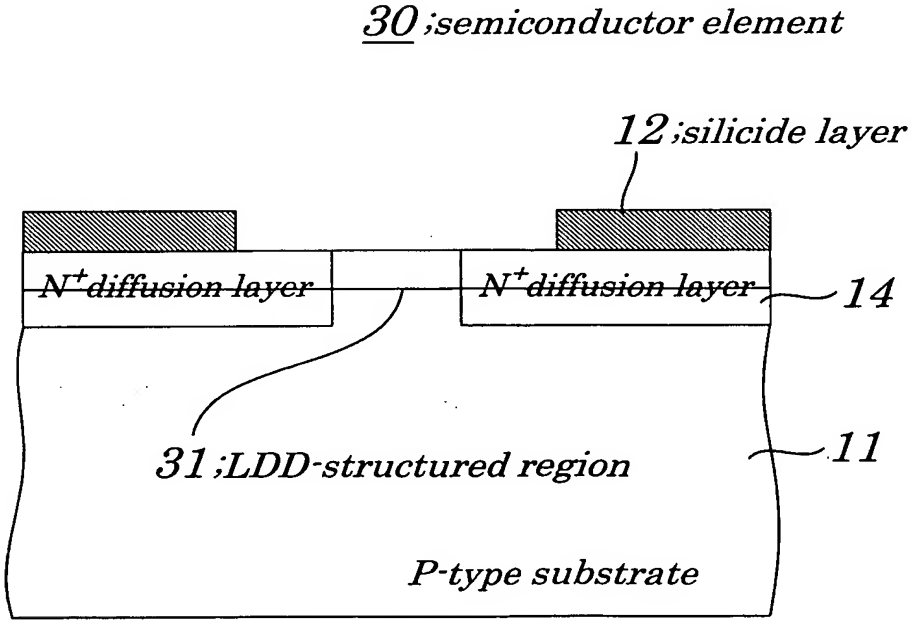
30;semiconductor element
12;silicide layer
N+diffusion layer
N+diffusion layer
14
31;LDD-structured region
11
P-type substrate

FIG.21

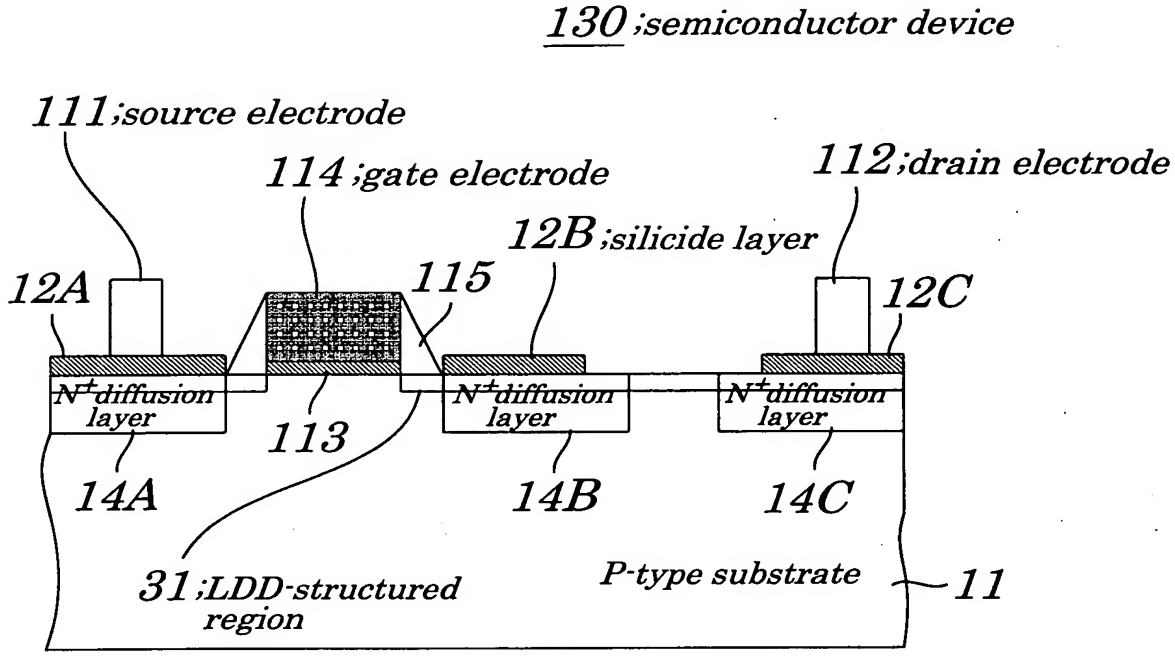
130;semiconductor device
111;source electrode
114;gate electrode
112;drain electrode
12B;silicide layer
12A
115
12C
N+diffusion layer
N+diffusion layer
N+diffusion layer
113
14A
14B
14C
31;LDD-structured region
P-type substrate
11

FIG.22

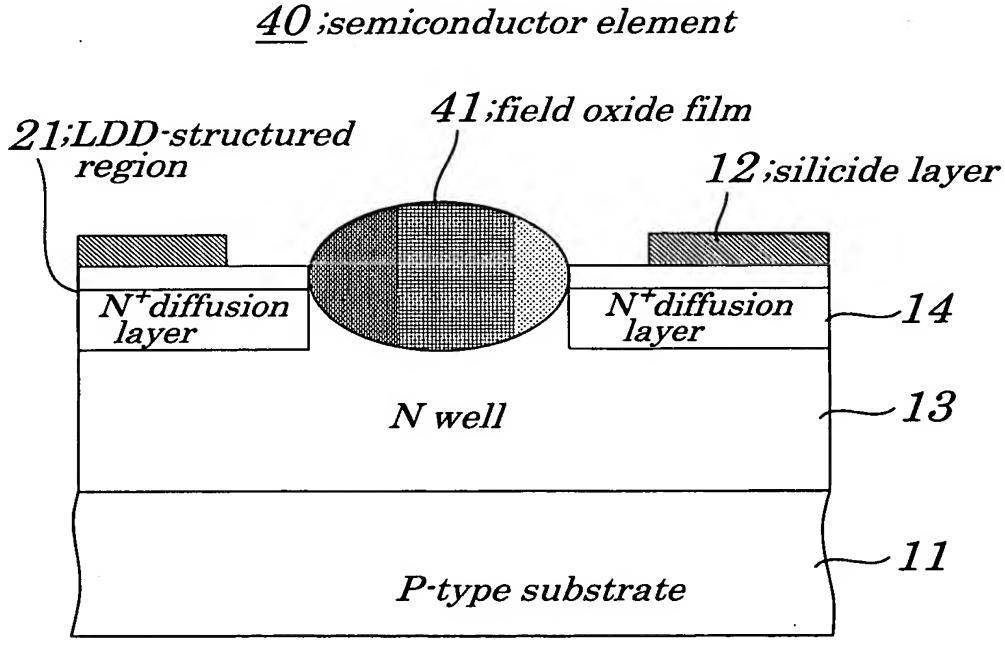
40;semiconductor element
41;field oxide film
21;LDD-structured region
12;silicide layer
N+diffusion layer
N+diffusion layer
14
N well
13
11
P-type substrate

FIG.23

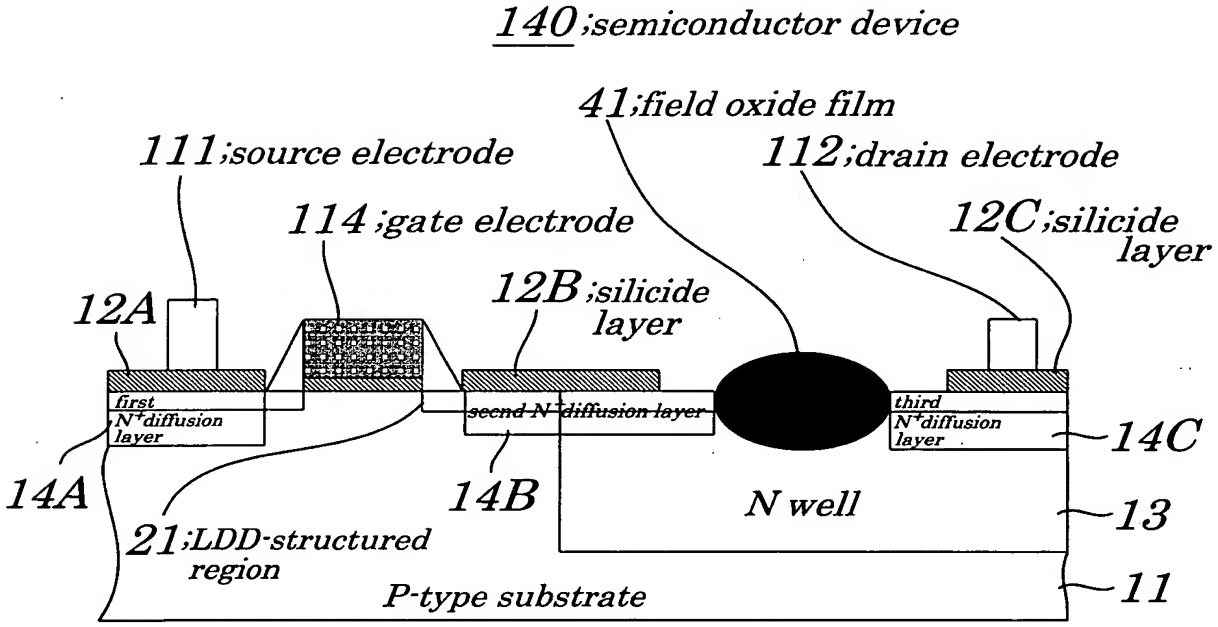
140;semiconductor device
41;field oxide film
111;source electrode
112;drain electrode
114;gate electrode
12C;silicide layer
12B;silicide layer
12A
first N+diffusion layer
second N+diffusion layer
third N+diffusion layer
14C
14A
14B
N well
13
21;LDD-structured region
P-type substrate
11

FIG.24

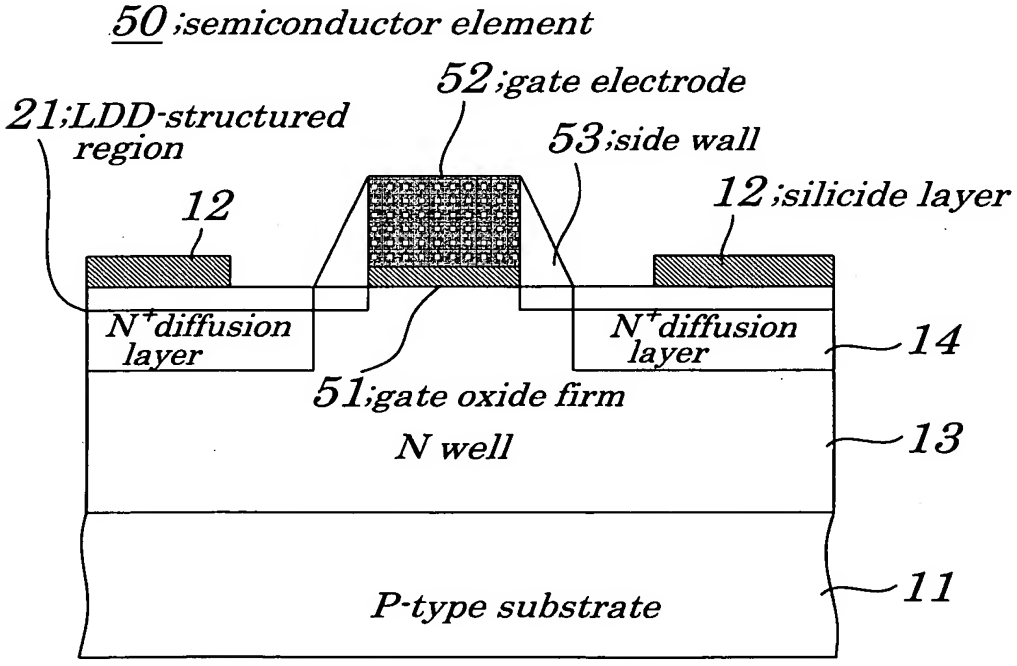
50;semiconductor element
52;gate electrode
21;LDD-structured region
53;side wall
12
12;silicide layer
N+diffusion layer
N+diffusion layer
14
51;gate oxide firm
N well
13
P-type substrate
11

FIG.25

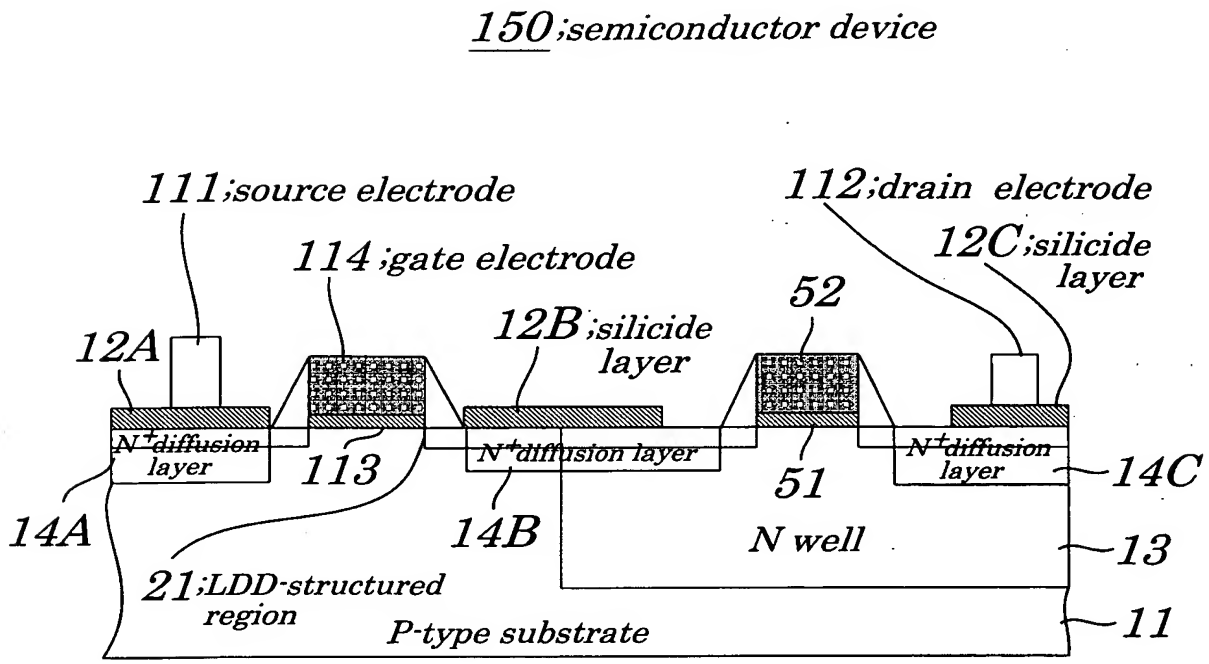

FIG.26 (PRIOR ART)

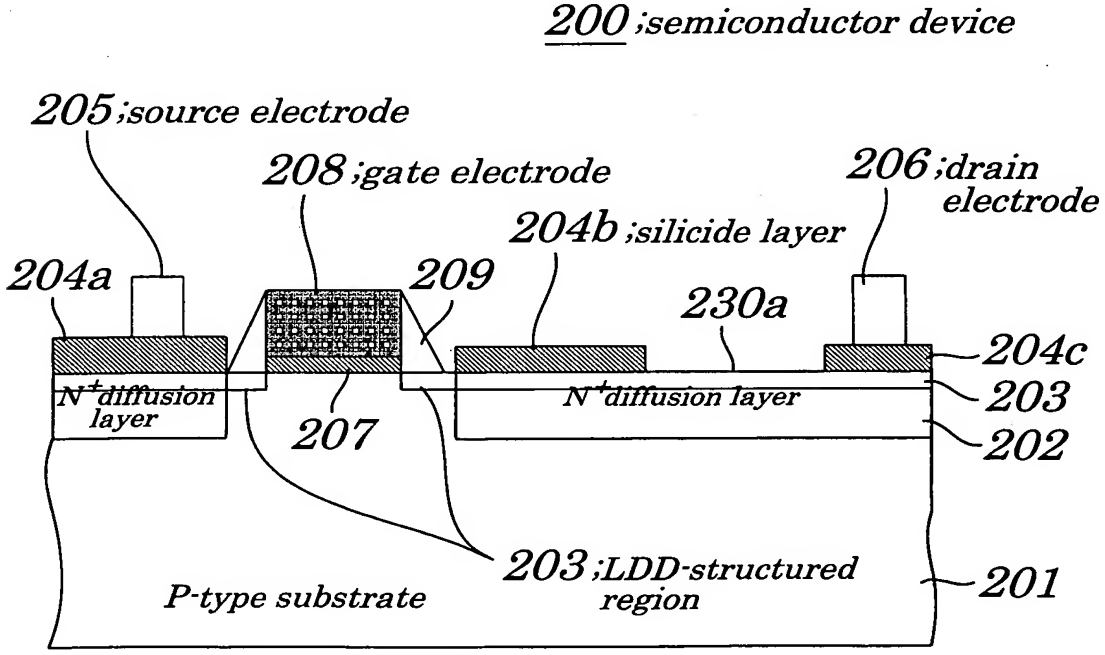

FIG.27 (PRIOR ART)

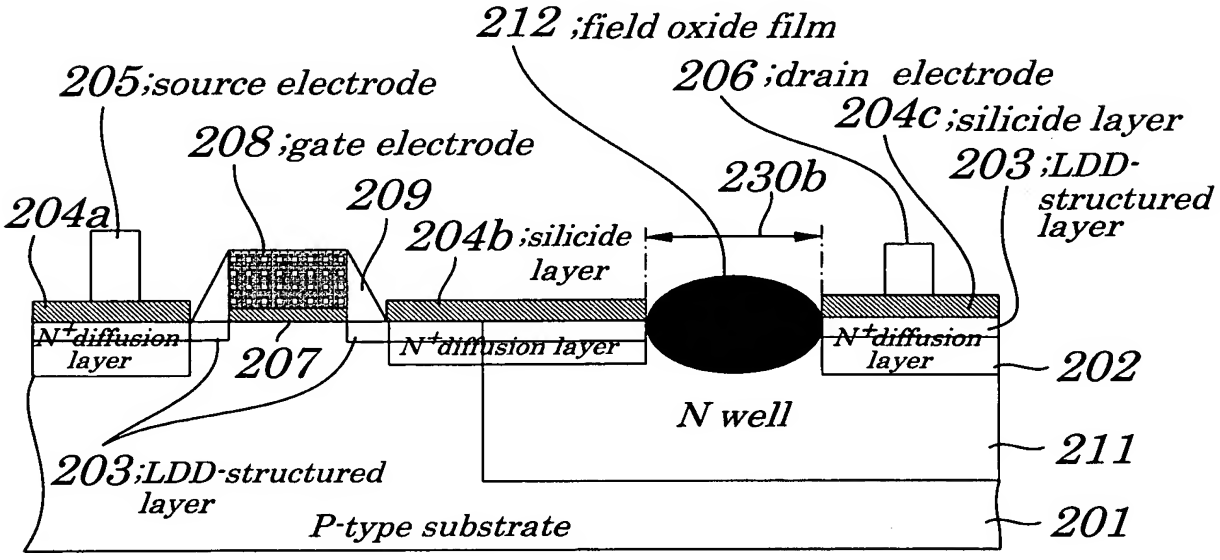

FIG.28 (PRIOR ART)

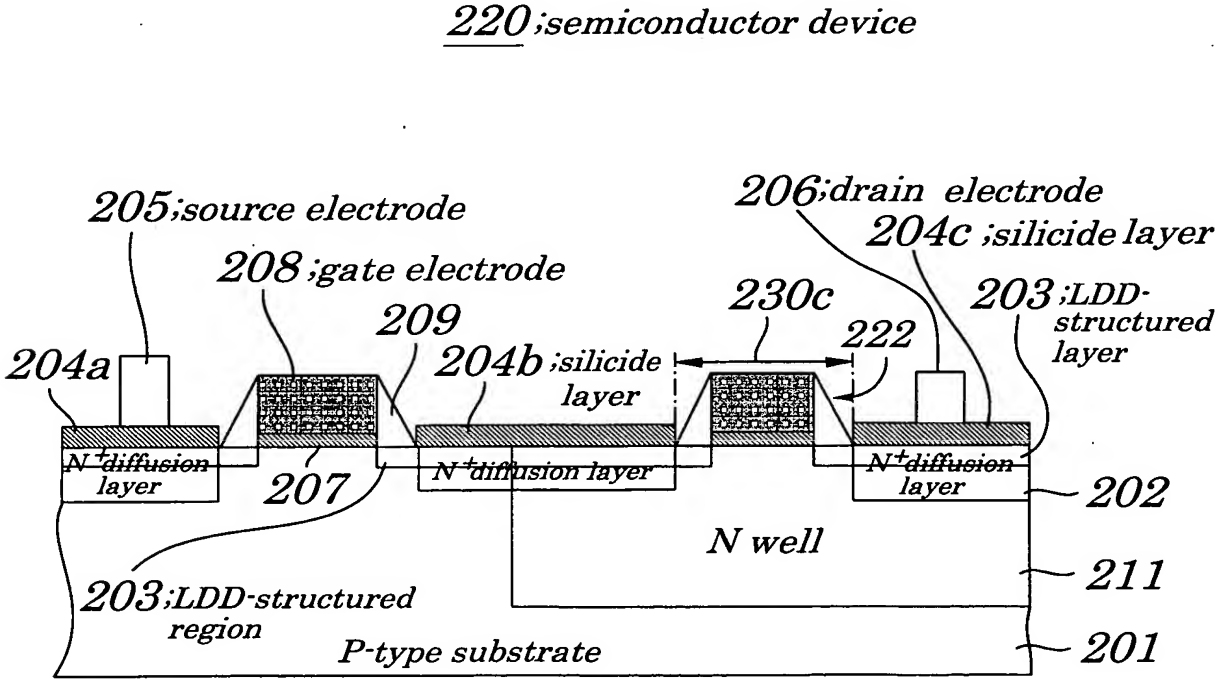

FIG.29A (PRIOR ART)

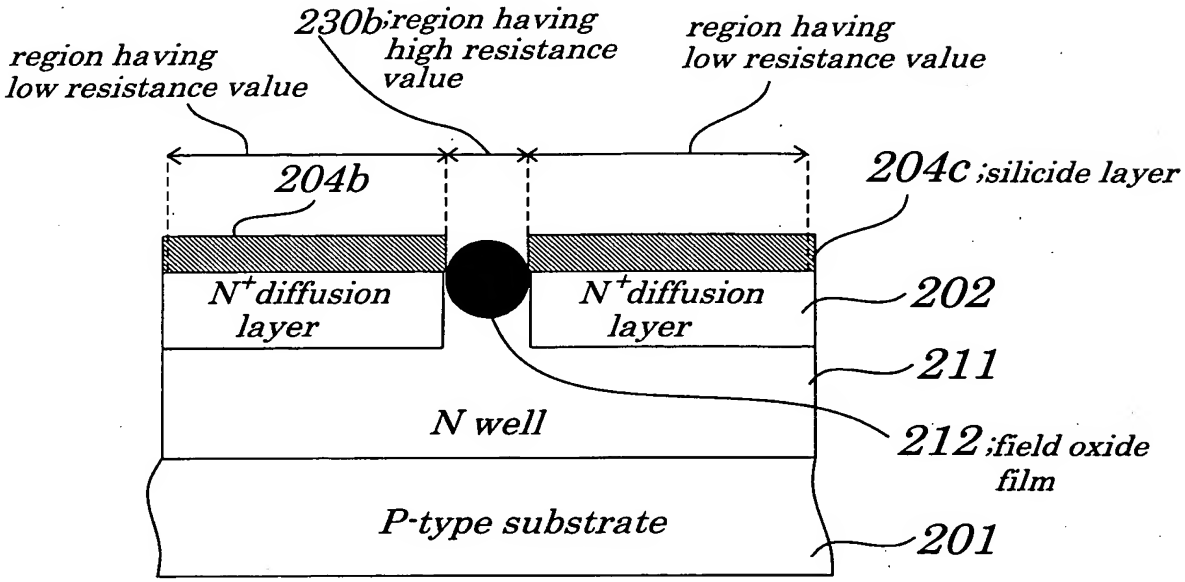

FIG.29B (PRIOR ART)